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RF3321

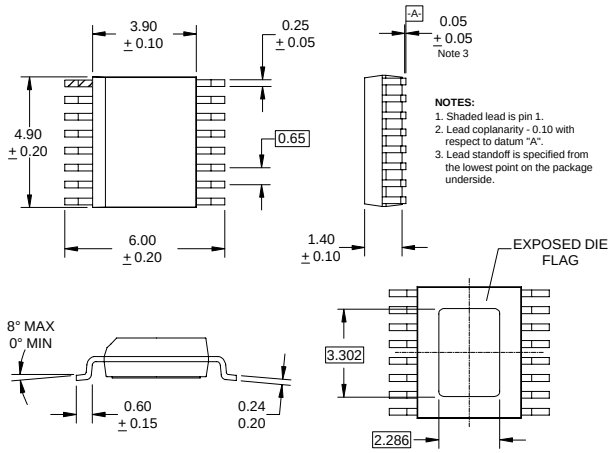
REVERSE PATH HIGH OUTPUT POWER
PROGRAMMABLE GAIN AMPLIFIER

Typical Applications

- Euro-DOCSIS/DOCSIS Cable Modems
- CATV Set-Top Boxes
- Telephony Over Cable
- Home Networks
- Automotive/Mobile Multimedia
- Coaxial and Twisted Pair Line Driver

Product Description

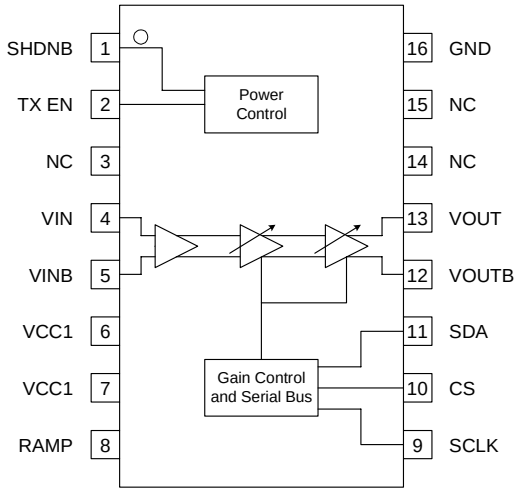
The RF3321 is a variable gain amplifier for use in CATV reverse path (upstream) applications. It is designed to be DOCSIS-compliant for use in cable modems. The gain control covers a 56dB range and is serially programmable via three-wire digital bus for compatibility with standard baseband chipsets. Amplifier shutdown and transmit disable modes are hardware-controlled. The device operates over the frequency band of 5MHz to 65MHz for use in current U.S. and European systems. The amplifier delivers up to +69dBmV at the output of the balun. Gain is controllable in accurate 1dB steps. The device is provided in a thermally enhanced, exposed die flag package.



Package Style: SSOP16 EDF Slug

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Differential Input and Output
- 31dB Maximum Voltage Gain
- -25dB Minimum Voltage Gain
- 5MHz to 65MHz Operation
- Sophisticated Power Management
- DOCSIS 1.1 RF Compliant

Ordering Information

RF3321	Reverse Path High Output Power Programmable Gain Amplifier
RF3321 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC1})	-0.5 to +5.5	V_{DC}
Supply Voltage (V_{CC2})	-0.5 to +7.5	V_{DC}
Input RF Level	12	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Humidity	80	%
Maximum Power Dissipation	0.5	W
Maximum T_J	150	°C

Caution! ESD sensitive device.

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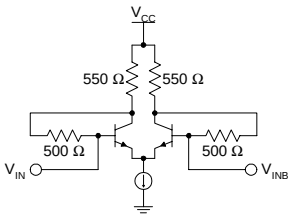
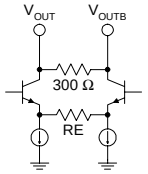
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC1}=5V, V_{CC2}=7V, TXEN=SHDNB=1, V_{IN}=38dBmV (rms) differential, output impedance=75Ω through a 2:1 transformer. Typical performance is at T_A=+25°C, V_{CC}=5V.
DC Specifications					
Supply Voltage 1 (VCC1)	4.75	5.0	5.25	V	Main chip supply
Supply Voltage 2 (VCC2)	6.65	7.0	7.35	V	Output stage supply
Supply Current					
Maximum Gain, SV1		85	100	mA	Gain Control Word=56, V_{CC2}=5V or 7V
Maximum Gain, SV2		135	150	mA	Gain Control Word=56, V_{CC2}=5V or 7V
Low Gain, SV1		75	90	mA	Gain Control Word<28, V_{CC2}=5V or 7V
Low Gain, SV2		55	70	mA	Gain Control Word<28, V_{CC2}=5V or 7V
Transmit Disable		25	35	mA	TXEN=0, V_{CC2}=5V or 7V
Shut Down		5		mA	SHDNB=0, V_{CC2}=5V or 7V
Logic High Voltage	2			V	
Logic Low Voltage			0.8	V	
Logic Leakage Current	-1		1	µA	
AC Specifications					
Voltage Gain					
Maximum	29	31		dB	Gain Control Word=56, V_{CC2}=5V or 7V
Minimum		-25	-23	dB	Gain Control Word=0, V_{CC2}=5V or 7V
Bandwidth		100		MHz	Intended operating range is 5MHz to 65MHz.
Maximum Input Level			40	dBmV(rms)	
Maximum Output Level			69	dBmV(rms)	Into 75Ω load at balun output (CW), V_{CC2}=7V
			65	dBmV	V_{CC2}=5V
Output Harmonic Distortion		-56	-50	dBc	Output Level=68dBmV (rms) (CW) Maximum Gain, V_{CC2}=5V or 7V
Output Step Size	0.8	1.0	1.1	dB	
Output Noise					
Maximum Gain		-35	-30	dBmV/ 160kHz	V_{CC2}=5V or 7V
Minimum Gain		-50	-45	dBmV/ 160kHz	V_{CC2}=5V or 7V
Transmit Disabled		-75	-70	dBmV/ 160kHz	TXEN=0, V_{CC2}=5V or 7V
TX EN Enable Time		0.5	1.0	µS	Time for gain to reach 99% of final value. See Note 1.
TX EN Transient Duration	2.4	3.0		µS	See Note 1.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
AC Specifications, cont'd					
Output Switching Transients					
Maximum Gain		10	20	mV_{P-P}	
Minimum Gain		5	7	mV_{P-P}	
Output Impedance		300		Ω	Chip output impedance is nominally 300Ω. Differential to single-ended output conversion to 75Ω is performed in a balun with a 2:1 turns ratio, corresponding to a 4:1 impedance ratio.
Input Impedance		75		Ω	Differential
Thermal					
$Theta_{JC}$		28		°C/W	

Note 1: The enable time is determined by the value of the capacitor on pin 8 (RAMP). A higher capacitor value will increase the enable time, but will reduce the transient voltage.

Pin	Function	Description	Interface Schematic
1	SHDNB	Chip shutdown pin. Forcing a logic low causes all circuits to switch off and gain settings to be lost.	
2	TX EN	Signal path enable pin. Logic high turns on signal path. Logic low turns off signal path, but leaves serial bus active.	
3	NC	Not connected.	
4	VIN	Input pin. This should be externally AC-coupled to signal source.	
5	VINB	Complementary input pin. This should be externally coupled to signal source. For single-ended use, this pin should be AC-coupled to ground.	See pin 4.
6	VCC1	This pin is connected to VCC1.	
7	VCC1	Same as pin 6.	
8	RAMP	External capacitor to ground controls start-up time.	
9	SCLK	Serial bus clock input.	
10	CS	Serial bus enable.	
11	SDA	Serial bus data input.	
12	VOUTB	Open collector output. Connect to VCC2 via balun primary.	
13	VOUT	Open collector output. Connect to VCC2 via balun primary.	See pin 12.
14	NC	Same as pin 3.	
15	NC	Same as pin 3.	
16	GND	Connect to ground.	
PKG BASE	GND	Die is mounted on a heat sink slug that should be connected to ground. Device grounds are internally bonded to the slug.	

Serial Bus Block Diagram

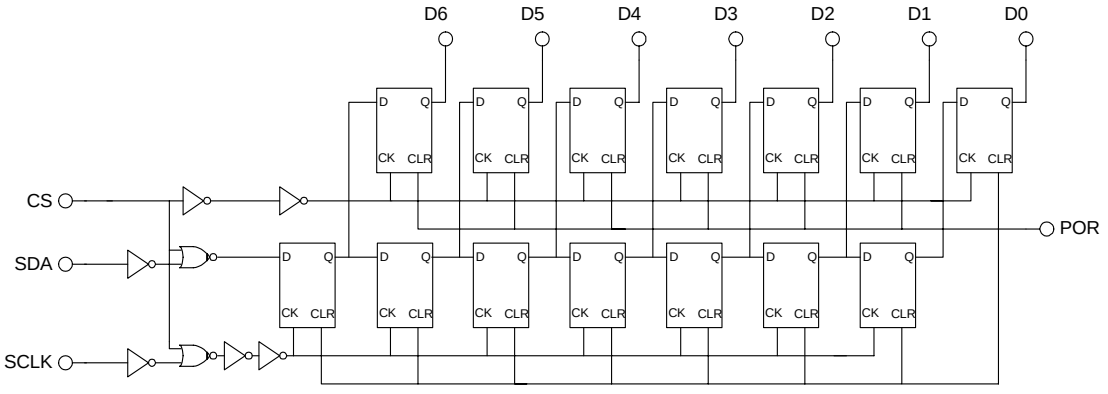


Table 1. Serial Interface Control Word Format

Bit	Mnemonic	Description
MSB 6	D6	Sleep Mode (Software Shutdown)
5	D5	Gain Control, Bit MSB
4	D4	Gain Control, Bit 4
3	D3	Gain Control, Bit 3
2	D2	Gain Control, Bit 2
1	D1	Gain Control, Bit 1
LSB 0	D0	Gain Control, Bit LSB

Serial Bus Timing Diagram

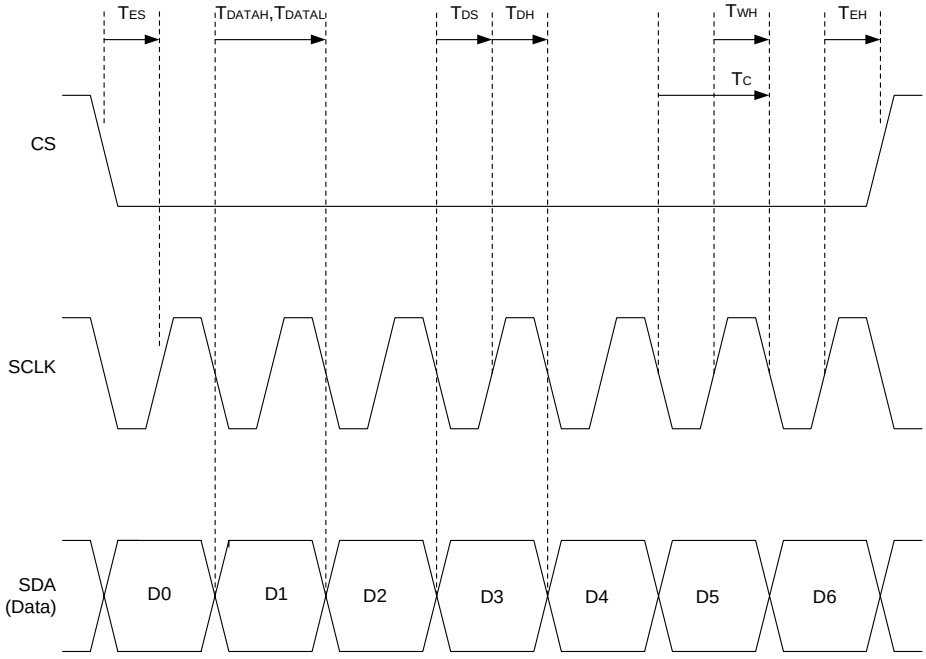


Table 2. Timing Data

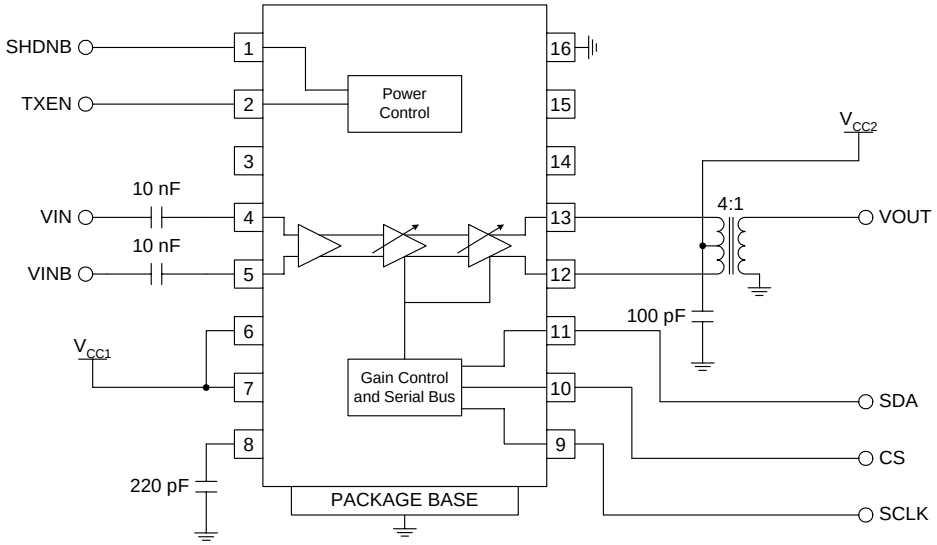
Parameter	Symbol	Min	Typ	Max	Units
SCLK Pulsewidth	T_{WH}	50			ns
SCLK Period	T_C	100			ns
Setup Time, SDA versus S CLK	T_{DS}	10			ns
Setup Time, CS versus S CLK	T_{ES}	10			ns
Hold Time, SDA versus S CLK	T_{DH}	20			ns
Hold Time, CS versus S CLK	T_{EH}	20			ns
SCLK Pulsewidth, High	T_{DATAH}	50			ns
SCLK Pulsewidth, Low	T_{DATAL}	50			ns

Table 3. Programming State

	TX	SHDND	MSB6
Enter Sleep Mode	X	H	L
Exit Sleep Mode	X	H	H*
Enter Shutdown	X	L	X
Exit Shutdown	X	H	H*
TX Enable	H	X	X
TX Disable	L	X	X

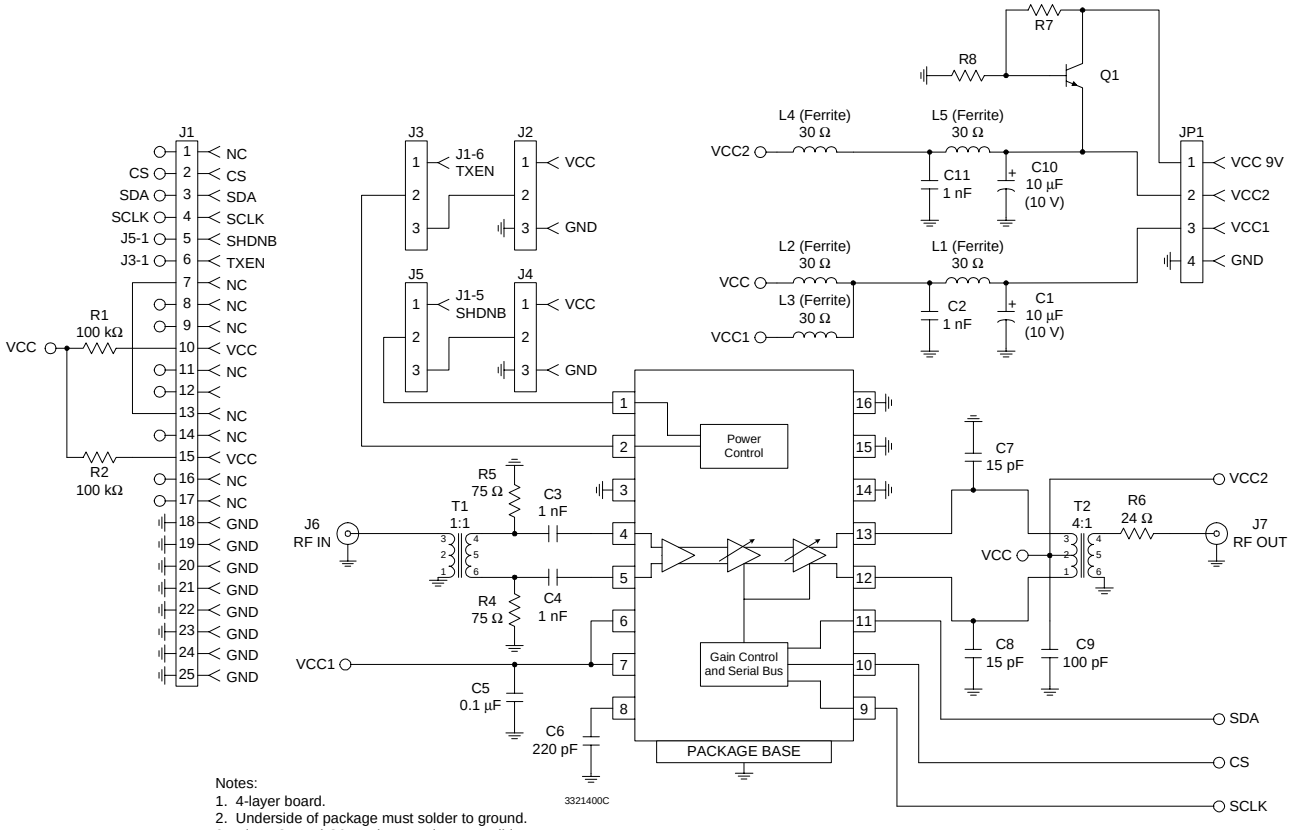
H=High Voltage Logic
L=Low Voltage Logic
X=Don't Care
*Gain Control Data Must be Re-Sent

Application Schematic



Evaluation Board Schematic

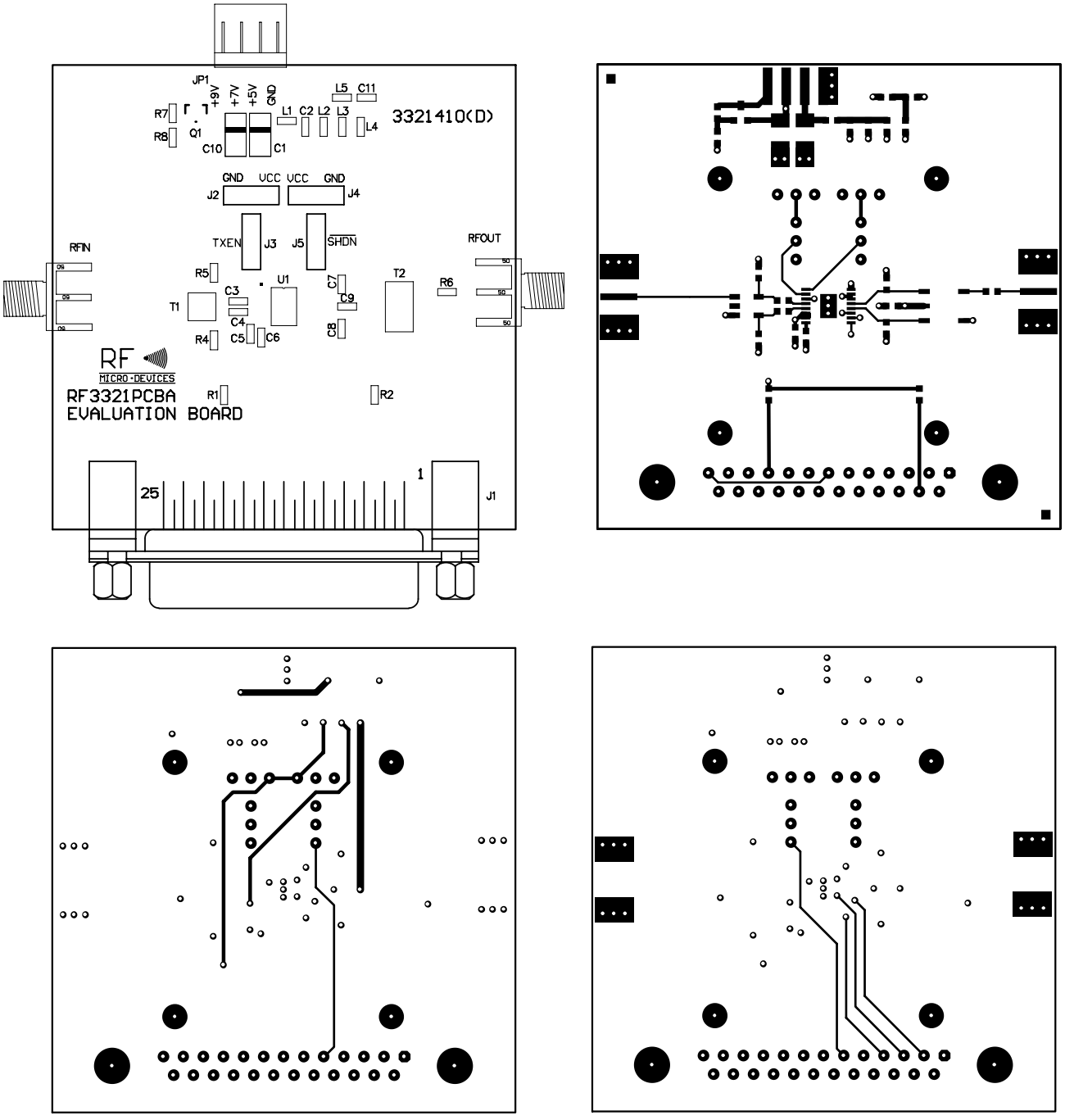
(Download Bill of Materials from www.rfmd.com.)



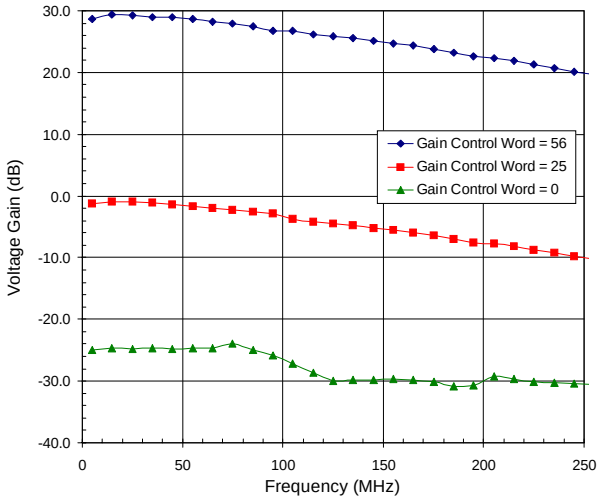
Notes:
1. 4-layer board.
2. Underside of package must solder to ground.
3. Place C5 and C6 as close to pin as possible.
4. C1 and C10 are tantalum, size code Y.
5. All other components are 0603 size.
6. Replace R6 with 0 Ω resistor if 75 Ω connector is used.

Evaluation Board Layout
Board Size 2.5” x 2.5”

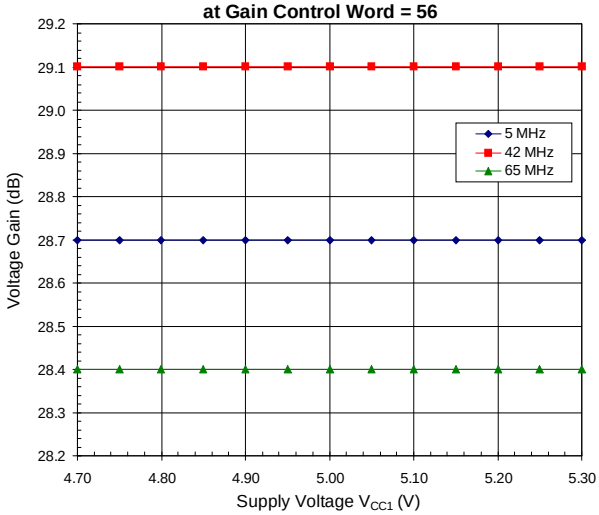
Board Thickness 0.058”, Board Material FR-4, Multi-Layer



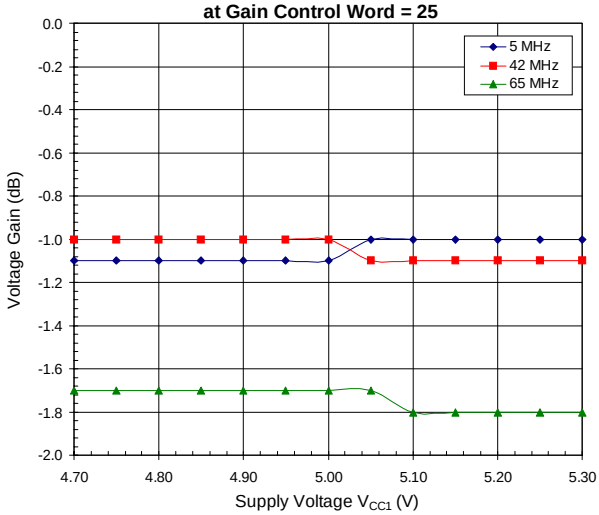
Gain versus Frequency



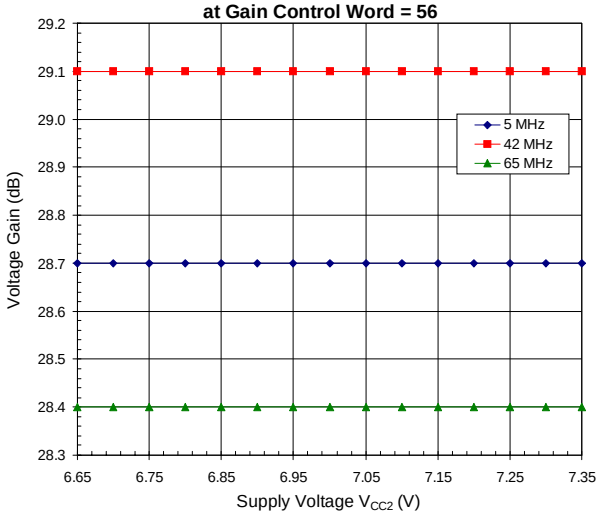
Gain versus Supply Voltage (V_{CC1}) at Gain Control Word = 56



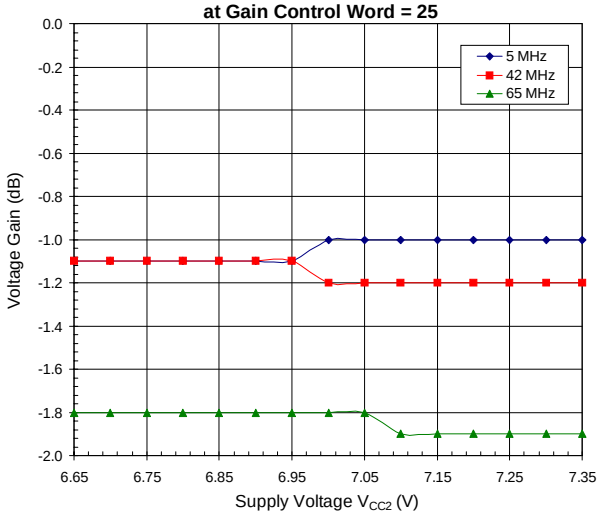
Gain versus Supply Voltage (V_{CC1}) at Gain Control Word = 25



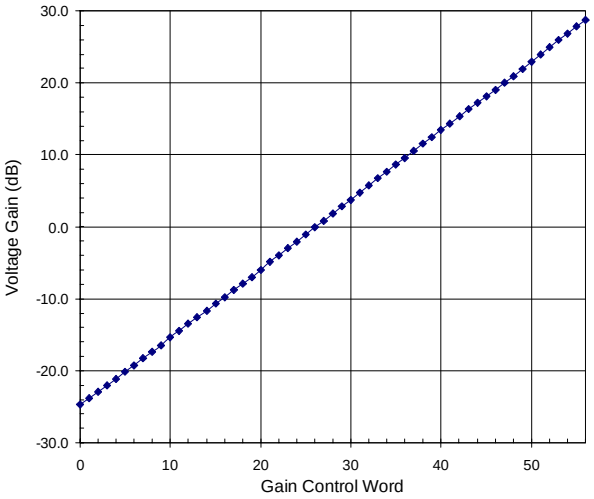
Gain versus Supply Voltage (V_{CC2}) at Gain Control Word = 56



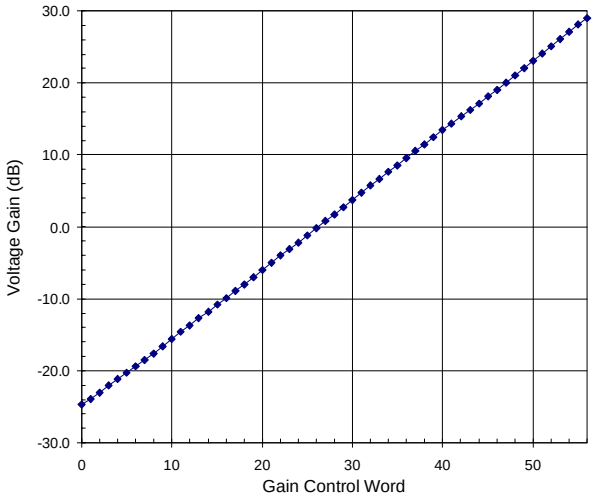
Gain versus Supply Voltage (V_{CC2}) at Gain Control Word = 25



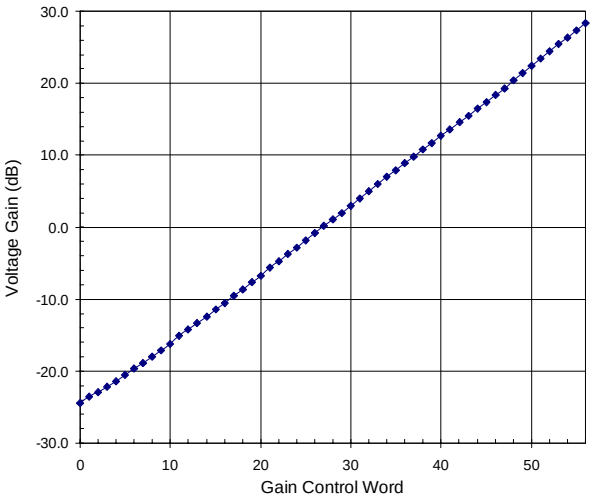
Gain versus Gain Control Word at 5 MHz



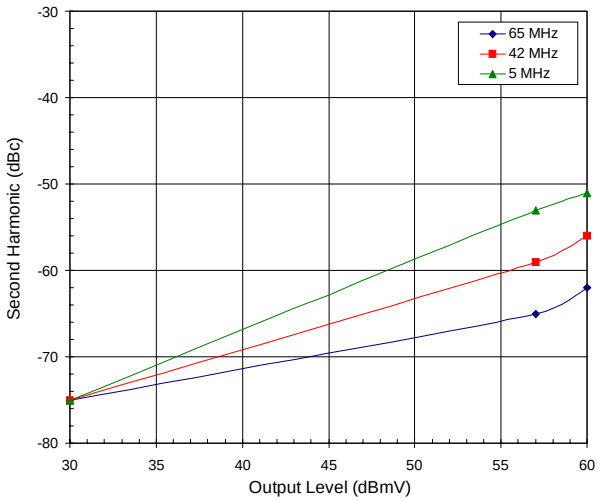
Gain versus Gain Control Word at 42 MHz



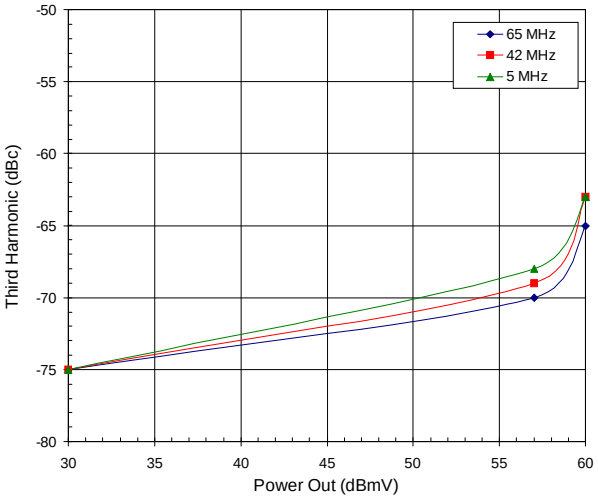
Gain versus Gain Control Word at 65 MHz

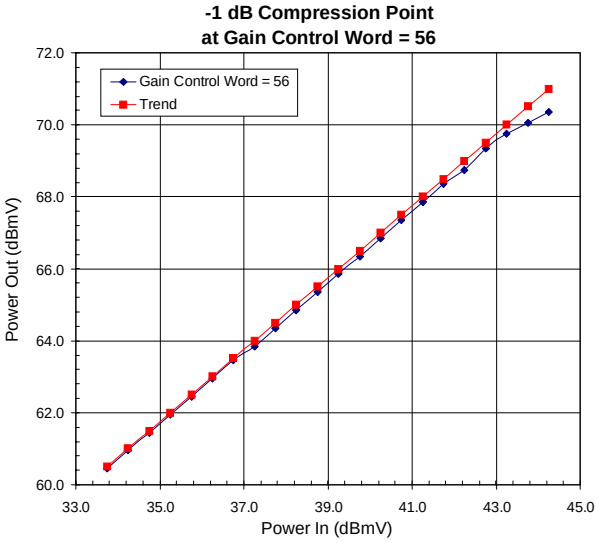


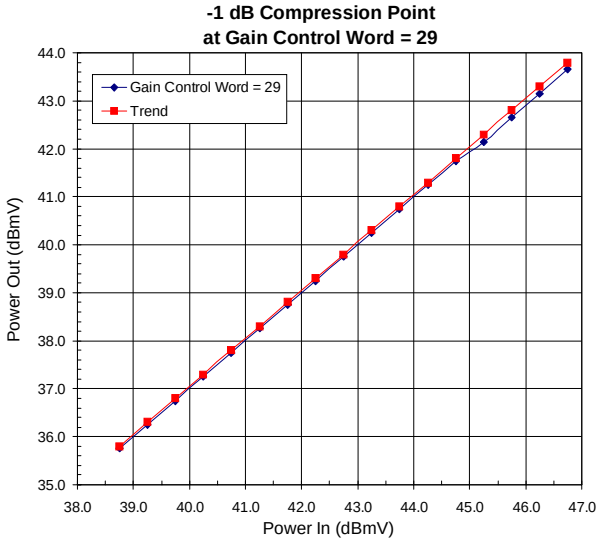
Second Harmonic versus Frequency and Output Level



Third Harmonic versus Frequency and Output Level




-1 dB Compression Point
at Gain Control Word = 56
Gain Control Word = 56
Trend
Power Out (dBmV)
Power In (dBmV)
72.0
70.0
68.0
66.0
64.0
62.0
60.0
33.0
35.0
37.0
39.0
41.0
43.0
45.0


-1 dB Compression Point
at Gain Control Word = 29
Gain Control Word = 29
Trend
Power Out (dBmV)
Power In (dBmV)
44.0
43.0
42.0
41.0
40.0
39.0
38.0
37.0
36.0
35.0
38.0
39.0
40.0
41.0
42.0
43.0
44.0
45.0
46.0
47.0

Evaluation Kit

General Description

The RF3321 PCBA is a fully assembled evaluation board of the RF3321 reverse path high output power programmable gain amplifier, useful for providing a demonstration of the RF3321's functionality. The RF3321 PCBA is a digitally controlled variable gain amplifier capable of driving a 75Ω source. The RF3321 is designed to send cable modem data with QPSK or QAM modulated format at frequencies between 5MHz and 65MHz. The gain is controlled by an 7-bit serial data word which adjusts the output gain from -25dB to +31dB.

The kit includes a fully functional evaluation board along with a serial data cable and software. The cable connects directly to the parallel port of a standard PC. The software is used to control the serially programmable gain through a simple, easy to understand user interface.

Input and output to the evaluation board is provided through 50Ω SMA connectors. The input and output of the evaluation board is matched to 50Ω and connected through a balun for single-ended operation. This allows easy connection to test equipment, but the evaluation board can easily be converted to a 75Ω input and output, or for differential input and output. The output circuit is matched using a 24Ω series resistor which is used to bring the load impedance up to 75Ω when using standard 50Ω test equipment. This will introduce a loss which must be accounted for in all measurements (see measurement section and evaluation board schematic for more detail.)

PCBA Details

Input Circuit

The input to the RF3321 is differential and the impedance is 75Ω; However, for ease of testing, the evaluation board has been changed to single-ended and the impedance has been matched to 50Ω. If a 75Ω input is required, simply replace the 50Ω SMA connector with a 75Ω F-style connector and remove R4 and R5.

Output Circuit

The output of the RF3321 is differential and the impedance is 300Ω. In normal applications this is converted into a single-ended 75Ω output using a 2:1 (voltage ratio) transformer with a center-tap on the secondary which supplies power to the output stage. The evaluation board is configured for use with 50Ω test equipment. This has been achieved with a 24Ω resistor in series with the output to increase the load seen by the device to 75Ω. This introduces a voltage loss of 3.5dB which must be accounted for in all measurements. Some spectrum analyzers have a setting to account for this method of 75Ω testing (e.g., on a Rhode & Schwartz spectrum analyzer the input can be set to '"75Ω RAZ" and the loss is accounted for automatically). A more accurate way of making this measurement is to use a 75Ω spectrum analyzer, or use a matching transformer or minimum loss pad. This ensures that the source impedance seen by the equipment is also 75Ω. If a 75Ω output is required, simply replace the 50Ω SMA connector (J7) with a 75Ω F-style connector and replace R5 with a 0Ω jumper. The evaluation board is tested with a Coilcraft balun; however, additional baluns may be used as long as care is taken in modifying the decoupling capacitors around the balun. These capacitors can greatly affect the harmonic suppression. Other baluns may be used but should be tested for second and third order harmonic suppression.

Transmit Enable

The transmit enable can be set to "continuous on" by placing the TXEN jumper in the up position (up position when viewing the top of the evaluation board with the 25-pin connector closest to the viewer) and placing the associated GND/VCC jumper in the "VCC" position. The transmit enable can be set to "continuous off" by placing the GND/VCC jumper in the "GND" position. If a computer controlled signal is used (J1), place the TXEN jumper in the down position.

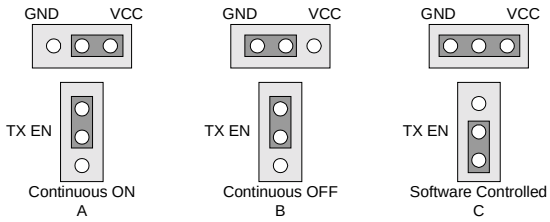


Figure 1. TX Enable Configuration

Shutdown Enable

Shutdown enable can be set to be “continuous on” (chip enabled) by placing the SHDN jumper in the up position and placing the associated GND/VCC jumper in the “VCC” position. Shutdown enable can be set to “continuous off” (chip disabled) by placing the associated GND/VCC jumper in the “GND” position. If a computer controlled signal is used (J1), place the SHDN jumper in the down position.

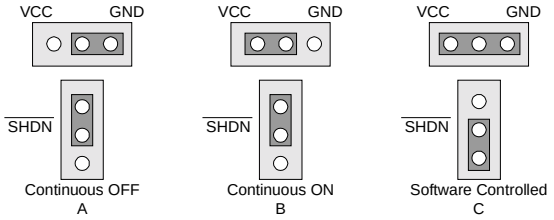


Figure 2. SHDN Enable Configuration

V_{CC} Settings

V_{CC1} should be set to 5.0V_{DC}.

V_{CC2} should be set to 7.0V_{DC}.

Evaluation Board Setup

Equipment Needed

- Signal Generator
- Spectrum Analyzer
- Power Supply (5.0V@300mA)
- RF3321 PCBA
- Serial Cable (included with kit)
- Standard PC
- Three-Wire Bus Software

Optional Equipment

- Variable Low-Pass or Band-Pass Filters
- Power Meter
- Second Signal Generator with Modulation for ACPR and IP2, IP3 Testing
- Arbitrary Wave Generator
- Two-Channel Oscilloscope

Software Setup

To install the software, you need a computer with the following.

- 133MHz Pentium processor
- 16MB RAM
- Hard Drive with 5MB free space
- Free 25-pin LPT port
- VGA Monitor

The software may be downloaded from www.rfmd.com by following these steps.

Select the “Product Support” tab;
Select “Evaluation Board Information”;
Select “RF3321”.

Unzip the file using WinZip 7.0 or higher (http://www.winzip.com). Unzip to a temporary directory and run RF3321.exe.

The 7-bit Gain Control Word (GCW) in the data latch determines the gain setting in the RF3321. The gain control data (SDA) load sequence is initiated by a falling edge on CS. The SDA is serially loaded (LSB first) into the 7-bit shift register at each rising edge of the clock. While CS is low, the data latch holds the previous data word allowing the gain level to remain unchanged. After seven clock cycles the new data word is fully loaded and CS is switched high. This enables the data latch and the loaded register data is passed to the gain control block with the updated gain value. Also at this CS transition, the internal clock is disabled, thus inhibiting new serial input data.

Software and Cable

Figure 3 shows the cable configuration. Connect the cable into the LPT1 port of the computer running the software. Connect the other end of the cable to the 25-pin connector of the evaluation board. Executing the software (RF3321.exe) will produce the screen shown in Figure 4. The user may set the gain of the evaluation board by sliding the gain control switch to the desired gain setting. Pressing the Preset Gain Value buttons automatically sets the gain of the unit to the value shown on the button. The Automatic Gain Adjustment when set to “Cycle” will automatically cycle through all of the gain steps (0-56) in seconds (at the rate set by the user). The user may place the unit in sleep, shutdown and transmit enable/disable modes by checking the corresponding box. The bit pattern being sent to the PCBA is shown at the bottom of the screen. See README_3321.txt file for proper pin/signal mapping for the 25 pin interface.

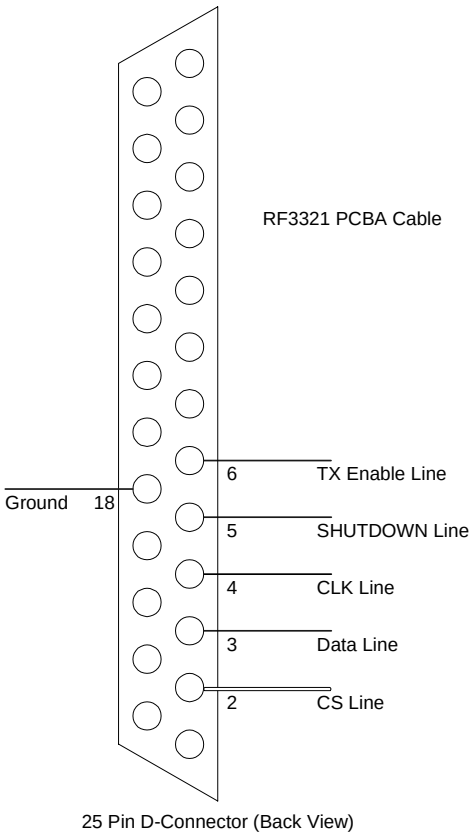


Figure 3. Cable Configuration

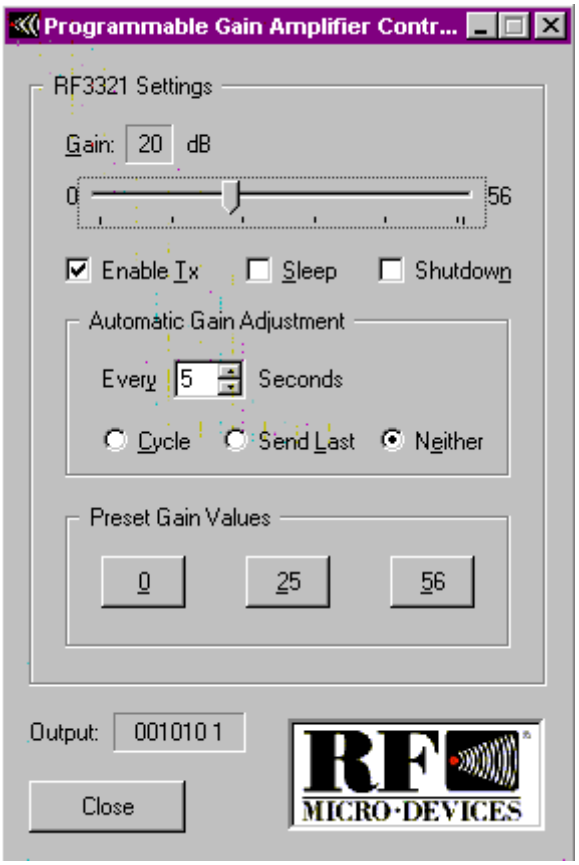


Figure 4. On-Screen Display

Hardware Setup

Gain and Harmonic Distortion Test Setup

To test the gain of the RF3321 PCBA, connect a low-pass or band-pass filter to the output of the signal generator. Use a filter just above the frequency you want to test. The filter is used to attenuate any harmonics output by the signal generator. Connect the signal generator to the power meter and measure the power. Compare with modulation enabled and disabled to make sure the meter was measuring average rather than peak power. No more than 0.2dB difference in power should be observed. An offset on the signal generator may be needed to match the level shown on the power meter. The signal generator should then be connected directly to a spectrum analyzer. Make sure the output of the signal generator is the same as the input read by the spectrum analyzer. Adjust the offset of the spectrum analyzer until the signal out is the same as the signal in on the spectrum analyzer. Turn off the RF and modulation. Check positioning of the jumpers on the board. Refer to the PCBA section of this application note to verify proper positions. Connect the output of the signal generator to J6: RFIN of the PCB. Connect J7: RFOUT to the spectrum analyzer. Ensure that you are accounting correctly for the losses in the 75Ω to 50Ω conversion at the output of the device; there is an output voltage loss of 3.5dB for the evaluation board in its standard configuration (see output stage circuit description). Connect one end of the serial cable into the computer and the other end into J1 of the PCB. Connect +5.0V_{DC} into V+ and ground into GND(JP1). Turn on the DC power and turn on RF from the signal generator. Set the GCW to 56 and make sure TX Enable is checked. The amplified signal should be displayed on the spectrum analyzer. The harmonics can also be viewed with this setup. As you change the GCW from 56 to 0 (in steps of one), there will be a 1dB change in the output of the PCB.

ACPR Test Setup

To test the ACPR of the RF3321 PCBA set modulation to:

- QPSK
- 2Bits/Sym
- 160ksps
- α=0.25
- PRBS-20bit Data

Set signal generator to:

- 45MHz,
- -13.0dBm output power,
- 0dB offset.

Connect 50MHz coaxial filter to output, then to output cable.

Zero and calibrate the power meter. Connect signal generator to power meter and set offset on signal generator until power meter reads -13.0dBm. Make sure power meter reads the same (±0.2dBm) with modulation enabled and disabled to verify power meter is measuring average power rather than peak power. Check positioning of the jumpers on the board. Refer to the PCBA section of this application note to verify proper positions. Connect the output of the signal generator to J6: RFIN of the PCB. Connect J7: RFOUT to the power meter. Connect one end of the serial cable into the computer and the other end into P1 of the PCB. Connect +5.0V_{DC} into V_{CC} and ground into GND. Turn on the DC power and turn on RF and modulation from the signal generator. Set the GCW to 56 and make sure TX Enable is checked. Measure and record channel power at RFOUT using the power meter (accounting for 75/50 conversion losses). Connect RFOUT to spectrum analyzer and adjust offset of the spectrum analyzer until the channel power displayed by the spectrum analyzer is equal to the channel power recorded in the previous step (Channel bandwidth = 200kHz). Now use the spectrum analyzer to measure relative ACP (this way the uncertainties in the spectrum analyzer power measurement are immaterial). The ACP is measured in 200kHz channel bandwidths at a 220kHz offset (i.e., from 20kHz to 220kHz outside the channel). As you increase the input power, you will notice a degradation of the ACP upper and lower bands.

Transmit Turn-On and Turn-Off Transients

Use an Arbitrary Waveform Generator set to a 3V square wave, 5% duty cycle, 120Hz as the input to the transmit enable. Set a signal generator to 10MHz, -13.0dbm output power, 0dB offset. Connect output of the signal generator to J6, RFIN of the PCB. Remove the TXEN jumper and connect the arbitrary wave generator square wave output to the center pin of the TXEN 3-pin header. Connect the output of the evaluation board to the oscilloscope (channel 1). Connect the TXEN signal from the arbitrary wave generator to channel 2 of the oscilloscope and trigger off of the rising edge. As the TXEN line is sent, the oscilloscope will trigger and capture the pulsed RFOUT signal. This will be displayed on the oscilloscope. Measure the amount of time between 90% of the TXEN turn-on to where the output signal reaches 90% of full turn-on. This is defined as the transmit turn-on time.

To measure the transient pulse, replace the signal generator input with a 50Ω terminator and repeat the steps above. Measure the size of the transient. This can be affected by the C_{RAMP} capacitor (C6), and the output balun and capacitor values around the balun. Larger values of C_{RAMP} will decrease the transient voltage and increase the TX enable time.

PCB Layout Considerations

The RF3321 Evaluation board can be used as a guide for the layout in your application. Care should be taken in laying out the RF3321 in other applications. The RF3321 will have similar results if the following guidelines are taken into consideration:

- Make sure underside of package is soldered to a good ground on the PCB.
- Move C2, C7, C8, and C9 as close to T1 as possible.
- Keep input and output traces as short as possible.
- Ensure a good ground plane by using multiple vias to the ground plane.
- Use a low noise power supply along with decoupling capacitors

Special Handling Information for Shrunk Small Outline Package (SSOP1-EPP) Products

These packages are considered JEDEC Level 5 for moisture sensitivity and require special handling to assure reliable performance.

The exposed copper slug on the bottom of the package improves both thermal and electrical performance. Since the RFIC is mounted directly on the thermal slug, and the slug is soldered directly on the PCB, the thermal resistance to the PCB is minimized. Also, the RF ground for the amplifier is established through this copper slug as it is soldered to the ground plane on the PCB. This offers the least inductance ground path available.

Care must be taken when soldering these packages to the PCB. They are currently considered JEDEC Level 5 for moisture sensitivity. Therefore the parts must be handled in a dry environment prior to soldering, as is specified in the JEDEC specification. Specifically, RFMD recommends the following procedure prior to assembly:

1. Dry-bake the parts at 125°C for 24 hours minimum. Note: the shipping tubes cannot withstand 125°C baking temperature.
2. Parts delivered on tape and reel are already dry-baked and dry-packed. These may be stored for up to one year, but must be assembled within 48 hours after opening the bag.
3. Assemble the dry-baked parts within two days of removal from the oven.
4. During this two-day period, the parts must be stored in humidity less than 60%.

IMPORTANT!
If the two-day period is exceeded, then this procedure must be repeated prior to assembly.